AMENDMENTS TO THE CLAIMS

Claims 1-9. (Cancelled)

10. (Original) A phase shifter circuit, comprising:

a circuit clock input terminal;

a multi-bit circuit input terminal;

a counter circuit having an input terminal coupled to the circuit clock input terminal and further having a multi-bit output terminal;

a first subtractor having a multi-bit input terminal coupled to the output terminal of the counter circuit and further having a multi-bit output terminal;

a first multiplexer circuit having a first multi-bit data input terminal coupled to the output terminal of the counter circuit, a second multi-bit data input terminal coupled to the output terminal of the first subtractor, a select terminal, and a multi-bit output terminal;

a comparator circuit having a first multi-bit input terminal coupled to the output terminal of the first multiplexer circuit, a second multi-bit input terminal coupled to the circuit input terminal, and an output terminal coupled to the select terminal of the first multiplexer circuit;

a second multiplexer circuit having a first multi-bit data input terminal coupled to the circuit input terminal, a second multi-bit data input terminal coupled to the output terminal of the counter circuit, a select terminal coupled to the output terminal of the comparator circuit, and an output terminal; and

a phase shifter having a clock input terminal coupled to the circuit clock input terminal, a multi-bit control terminal coupled to the output terminal of the second multiplexer circuit, and an output terminal.

11. (Original) The phase shifter circuit of Claim 10, further comprising a second subtractor coupled between the output terminal of the counter circuit and the first data input terminal of the first multiplexer circuit, and between the output terminal of the counter circuit and the second data input terminal of the second multiplexer circuit, wherein the second subtractor subtracts a smaller number than the first subtractor.

12. (Original) The phase shifter circuit of Claim 10, further comprising an overflow prevention circuit coupled between the output terminal of the comparator circuit and the select terminal of the first multiplexer circuit, the overflow prevention circuit having an additional input terminal coupled to the output terminal of the counter circuit.

13. (Original) The phase shifter circuit of Claim 10, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is greater than a value at the first input terminal of the comparator circuit.

14. (Original) The phase shifter circuit of Claim 10, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is not less than a value at the first input terminal of the comparator circuit.

Claims 15-23. (Cancelled)